I/WE CLAIM:

Sub A1 1. A digital frequency detector for detecting a difference between a frequency of an oscillator output signal and a frequency of a data signal, the digital frequency detector comprising:

a) first digital sample means for sampling the oscillator output signal at a timing of the data signal to generate a first beat signal;

b) second digital sample means for sampling a quadrature clock signal at a timing of the data signal to generate a second beat signal; and

c) third digital sample means for sampling the second beat signal at a timing of the first beat signal to generate a frequency error signal.

2. A digital frequency detector as claimed in claim 1, wherein a frequency of the quadrature clock signal is substantially identical to that of the oscillator output signal, and a phase difference between the quadrature clock signal and the oscillator output signal is between about 45° and 135°.

3. A digital frequency detector as claimed in claim 2, wherein a phase difference between the quadrature clock signal and the oscillator output signal is about 90°.

4. A digital frequency detector as claimed in claim 1, wherein the first sample means comprises:

a) a first pair of digital latch circuits respectively adapted to sample the oscillator

output signal on rising and falling edges of the data signal; and

b) a first multiplexor adapted to selectively switch between respective outputs of the first pair of digital latch circuits on transitions of the data signal.

5. A digital frequency detector as claimed in claim 1, wherein the second sample means comprises:

a) a second pair of digital latch circuits respectively adapted to sample the quadrature clock signal on rising and falling edges of the data signal; and

b) a second multiplexor adapted to selectively switch between respective outputs of the second pair of digital latch circuits on transitions of the data signal.

6. A digital frequency detector as claimed in claim 1, wherein the frequency error signal is a differential signal comprising a complementary pair of first and second error signals, a difference between values of the first and second error signals indicating a frequency difference between the recovered clock signal and the data signal.

7. A digital frequency detector as claimed in claim 6, wherein the third sample means comprises:

a) a first digital flip-flop circuit adapted to sample the second beat signal on rising edges of the first beat signal;

b) a second digital flip-flop circuit adapted to sample the second beat signal on falling edges of the first beat signal;

c) a first logic gate adapted to output the first error signal when both the first beat signal and an output of the first digital flip-flop circuit are at a logical high level; and

d) a second logic gate adapted to output the second error signal when the first beat signal is at a logical low level and an output of the second digital flip-flop circuit is at a logical high level.

8. A digital frequency detector as claimed in claim 7, wherein the third sample means further comprises a digital delay circuit adapted to delay the first beat signal with respect to the second beat signal by a predetermined delay period, whereby a delayed first beat signal is supplied to the first and second digital flip-flop circuits and the first and second logic gates.

9. A digital frequency detector as claimed in claim 8, wherein the predetermined delay period is sufficiently long to permit the second beat signal to settle at respective inputs of the first and second digital flip-flop circuits.

10. A digital frequency detector as claimed in claim 9, wherein the predetermined delay period is less than a period of the oscillator output signal.

11. A digital frequency detector as claimed in claim 1, further comprising data-lock indicator means for generating a lock-indicator signal indicative of a frequency-lock condition between the oscillator output signal and the data signal.

12. A digital frequency detector as claimed in claim 11, wherein the data lock indicator means comprises:

a) frequency counter means for quantitatively determining a frequency difference between the oscillator output signal and the data signal, and adapted to generate a threshold indicator signal indicative of whether the frequency difference is greater or less than a predetermined threshold; and

b) a state machine adapted to debounce the threshold indicator signal to generate the lock-indicator signal.

13. A digital frequency detector as claimed in claim 12, wherein the frequency counter means comprises:

a) a counter for counting, during a predetermined sample period, a number of transitions of either one of the second beat signal and a third beat signal;

b) comparing means for comparing the counted number of transitions to a predetermined limit value, and for generating the threshold indicator signal indicative of a result of the comparison;

the predetermined threshold being defined as a function of the predetermined sample period and the predetermined limit value.

14. A digital frequency detector as claimed in claim 13, wherein the third beat signal is generated by a third multiplexor adapted to alternately select respective outputs of a pair of digital flip-flop circuits at a timing of transitions of the first beat signal, the pair of digital flip-flop circuits being adapted to sample the second beat signal on respective rising and falling edges of the first beat signal.

15. A digital frequency detector as claimed in claim 13, wherein the comparing means is adapted to generate a value of the threshold-indicator signal indicative of an in-lock condition when the counted number of transitions is less than the predetermined limit value, and is adapted to generate a value of the threshold-indicator signal indicative of an out-of-lock condition when the counted number of transitions is equal to or greater than the predetermined limit value.

16. A digital frequency detector as claimed in claim 15, wherein the sample period is adjustable to control the threshold value.

17. A digital frequency detector as claimed in claim 14, wherein the counter means comprises:

a) a first digital edge detector circuit responsive to the third multiplexor to generate an enable signal at a timing corresponding to transitions of the third beat signal;

b) a second digital edge detector circuit adapted to generate a reset signal at a timing corresponding to transitions of a sample clock; and

c) a digital counter circuit adapted to count cycles of the enable signal and to generate a pulse count signal indicative of the number of pulses of the enable signal counted between reception of consecutive pulses of the reset signal.

18. A digital frequency detector as claimed in claim 17, wherein the comparing means comprises a magnitude detector adapted to compare the counted number of pulses to the predetermined limit value, and to generate the threshold-indicator signal indicative of whether the number of pulses counted during the predetermined sample period is greater or less than the predetermined limit value.

19. A digital frequency detector as claimed in claim 18, wherein the comparing means further comprises a latch adapted to sample the comparison signal at a timing of the predetermined sample period to generate the lock-indicator signal.

20. A digital frequency detector as claimed in claim 12, wherein the state machine is adapted to:

a) sample successive values of the lock-indicator signal; and

i) transition to a DVIL state when a density of sampled values of the lock-indicator signal indicative of an out-of-lock condition exceeds a predetermined density tolerance; and

ii) transition to a DVIH state if a predetermined number of consecutive sampled

values of the lock-indicator signal are indicative of an in-lock condition.

21. A digital frequency detector as claimed in claim 20, wherein the predetermined density tolerance is 50%.

22. A digital frequency detector as claimed in claim 20, wherein the predetermined number is 1.

23. A digital frequency detector as claimed in claim 11, wherein the data lock indicator means is a fixed window phase lock indicator adapted to generate the lock-indicator signal on a basis of a proportion of time, in relation to the predetermined sample period, for which the second beat signal is at a logical-low level.

24. A digital frequency detector as claimed in claim 23, wherein the fixed window phase lock indicator comprises:

a) means for generating a reset signal at a timing of the predetermined sample period; and

b) an N-bit counter adapted to:

i) count bits of the oscillator output signal while the second beat signal is at a logical-low level, and accumulate the count in an N-bit counter;

ii) generate an over-flow signal indicative of an over-flow state of the N-bit counter; and

iii) reset a counted number of bits to zero upon receipt of the reset signal.

25. A digital frequency detector as claimed in claim 24, wherein the means for generating a reset signal comprises a 2^M frequency divider adapted to generate the reset signal by frequency-division of the oscillator output signal.

26. A digital frequency detector as claimed in claim 25, wherein values of N and M are selected to provide desired noise-rejection properties of the data lock indicator means.

27. A digital frequency detector as claimed in claim 24, wherein the fixed window phase lock indicator is adapted to assert a value of the lock-indicator signal indicative of an out-of-lock condition when a value of the over-flow signal indicates that the N-bit counter is in an over-flow state, and otherwise assert a value of the lock-indicator signal indicative of an in-lock condition.

28. A digital frequency detector as claimed in claim 27, wherein the fixed window phase lock indicator further comprises:

a) a third digital flip-flop circuit adapted to sample the over-flow signal at a timing of the reset signal; and

b) a logical-NOR gate adapted to assert a value of the lock-indicator signal corresponding to a value of one of the over-flow signal and an output of the third digital flip-flop circuit.

29. A digital frequency detector as claimed in claim 11, wherein the data lock indicator means is a sliding

window phase lock indicator adapted to generate the lock-indicator signal on a basis of a series of N consecutive samples of the second beat signal.

30. A digital frequency detector as claimed in claim 29, wherein the sliding window phase lock indicator is adapted to assert a value of the lock-indicator signal indicative of an out-of-lock condition if at least 2 out of N+1 consecutive samples of the second beat signal are at a logical low value, and assert a value of the lock-indicator signal indicative of an in-lock condition if at least N consecutive samples of the second beat signal are at a logical high value.

31. A digital frequency detector as claimed in claim 29, wherein the sliding window data frequency lock indicator comprises:

a) an input digital flip-flop circuit adapted to sample the second beat signal at a timing of a predetermined sample period;

b) an N-bit shift register connected to the input digital flip-flop circuit and adapted to store N consecutive samples of the second beat signal;

c) a first logic gate adapted to assert a high value of a first gate output signal when at least one of the N bits of the shift register, and an output of the input digital flip-flop circuit are at a low value;

d) a second logic gate adapted to assert a high value of a second gate output signal when all N bits of the shift register are at a high value; and

e) an output digital flip-flop circuit adapted to assert a value of the lock-indicator signal based on the first and second gate output signals.

32. A system for recovering a clock signal from a data signal, comprising:

a) an oscillator adapted to generate an oscillator output signal;

b) first detecting means for obtaining a course frequency-lock condition between the data signal and a recovered clock signal;

c) second detecting means for obtaining a phase-locked condition between the data signal and the recovered clock signal;

d) lock-detecting means responsive to the first detecting means for detecting an out-of-lock condition between the data signal and the recovered clock signal; and

e) control means responsive to the lock-detecting means and adapted to control the oscillator to generate an oscillator output signal on the basis of the first detecting means during an out-of-lock condition, and otherwise to generate the oscillator output signal on the basis of the second detecting means.

33. A system as claimed in claim 32, wherein the second detecting means comprises a phase detector adapted to generate a phase error signal indicative of a detected phase difference between the data signal and the oscillator output signal.

34. A system as claimed in claim 32, wherein the first detecting means comprises a digital frequency detector adapted to generate a frequency error signal indicative of a detected frequency difference between the data signal and the oscillator output signal.

Sub A17

35. A system as claimed in claim 34, wherein the lock-detecting means comprises a frequency lock detector responsive to the digital frequency detector and adapted to generate a lock-indicator signal indicative of a frequency-lock condition between the data signal and the oscillator output signal.

36. A system as claimed in claim 35, wherein the control means comprises:

a) a state machine responsive to the lock-indicator signal and adapted to generate a control signal; and

b) selection means responsive to the control signal and adapted to selectively enable control of the oscillator by either the first or second detector means.

37. A system as claimed in claim 34, wherein the digital frequency detector comprises:

a) first digital sample means for sampling the oscillator output signal at a timing of the data signal to generate a first beat signal;

b) second digital sample means for sampling a quadrature clock signal at a timing of the data signal to generate a second beat signal; and

c) third digital sample means for sampling the second beat signal at a timing of the first beat signal to generate a frequency error signal.

Sub A17

38. A system as claimed in claim 37, wherein a frequency of the quadrature clock signal is substantially identical to that of the oscillator output signal, and a phase difference between the quadrature clock signal and the oscillator output signal is between about 45° and 135°.

39. A system as claimed in claim 38, wherein a phase difference between the quadrature clock signal and the oscillator output signal is approximately 90°.

40. A system as claimed in claim 37, wherein the first sample means comprises:

a) a first pair of digital latch circuits respectively adapted to sample the oscillator output signal on rising and falling edges of the data signal; and

b) a first multiplexor adapted to selectively switch between respective outputs of the first pair of digital latch circuits on transitions of the data signal.

41. A system as claimed in claim 37, wherein the second sample means comprises:

a) a second pair of digital latch circuits respectively adapted to sample the quadrature clock signal on rising and falling edges of the data signal; and

b) a second multiplexor adapted to selectively switch between respective outputs of the second pair of digital latch circuits on transitions of the data signal.

42. A system as claimed in claim 37, wherein the frequency error signal is a differential signal comprising a complementary pair of first and second error signals, a difference between values of the first and second error signals indicating a frequency difference between the recovered clock signal and the data signal.

43. A system as claimed in claim 42, wherein the third digital sample means comprises:

a) a first digital flip-flop circuit adapted to sample the second beat signal on rising edges of the first beat signal;

b) a second digital flip-flop circuit adapted to sample the second beat signal on falling edges of the first beat signal;

c) a first logic gate adapted to output the first error signal when both the first beat signal and an output of the first digital flip-flop circuit are at a logical high level; and

d) a second logic gate adapted to output the second error signal when the first beat signal is at a logical low level and an output of the second digital flip-flop circuit is at a logical high level.

44. A system as claimed in claim 43, wherein the third digital sample means further comprises a digital

delay circuit adapted to delay the first beat signal with respect to the second beat signal by a predetermined delay period, whereby a delayed first beat signal is supplied to the first and second digital flip-flop circuits and the first and second logic gates.

45. A system as claimed in claim 44, wherein the predetermined delay period is sufficiently long to permit the second beat signal to settle at respective inputs of the first and second digital flip-flop circuits.

46. A system as claimed in claim 45, wherein the predetermined delay period is less than a period of the oscillator output signal.

47. A system as claimed in claim 32, wherein the lock-detecting means comprises:

a) frequency counter means for quantitatively determining a frequency difference between the oscillator output signal and the data signal, and generating a threshold indicator signal indicative of whether the frequency difference is greater or less than a predetermined threshold value; and

b) a state machine adapted to debounce the threshold indicator signal to generate the lock-indicator signal.

48. A system as claimed in claim 47, wherein the frequency counter means comprises:

a) a counter for counting, during a predetermined sample period, a number of transitions of either one of the second beat signal and a third beat signal;

b) comparing means for comparing the counted number of transitions to a predetermined limit value, and for generating the threshold indicator signal indicative of a result of the comparison;

the predetermined threshold value being defined by a function of the predetermined sample period and the predetermined limit value.

49. A system as claimed in claim 48, wherein the third beat signal is generated by a third multiplexor adapted to alternately select respective outputs of each of the first and second digital flip-flop circuits at a timing of transitions of the first beat signal.

50. A system as claimed in claim 48, wherein the comparing means is adapted to generate a value of the threshold-indicator signal indicative of an in-lock condition when the counted number of transitions is less than the predetermined limit value, and is adapted to generate a value of the threshold-indicator signal indicative of an out-of-lock condition when the counted number of transitions is equal to or greater than the predetermined limit value.

51. A system as claimed in claim 50, wherein the sample period can be adjusted.

52. A system as claimed in claim 48, wherein the frequency counter means comprises:

a) a first digital edge detector circuit responsive to the fourth sample means to generate an enable signal at a timing corresponding to transitions of the third beat signal;

b) a second digital edge detector circuit adapted to generate a reset signal at a timing corresponding to transitions of a sample clock; and

c) a digital counter circuit adapted to count pulses of the enable signal and to generate a pulse count signal indicative of the number of pulses counted between reception of consecutive pulses of the reset signal.

53. A system as claimed in claim 52, wherein the comparing means comprises a magnitude detector adapted to compare the counted number of pulses to a predetermined threshold, and to generate the threshold-indicator signal indicative of whether the number of cycles counted during the predetermined sample period is greater, equal to or less than the predetermined limit value.

54. A system as claimed in claim 53, wherein the comparing means further comprises a latch adapted to sample the comparison signal at a timing of the predetermined sample period to generate the lock-indicator signal.

55. A system as claimed in claim 47, wherein the state machine comprises monitor means adapted to sample

successive values of the lock-indicator signal, the state machine being adapted to:

a) transition to a DVIL state when a density of sampled values of the lock-indicator signal indicative of an out-of-lock condition exceeds a predetermined density tolerance; and

b) transition to a DVIH state if a predetermined number of consecutive sampled values of the lock-indicator signal are indicative of an in-lock condition.

56. A system as claimed in claim 55, wherein the predetermined density tolerance is 50%.

57. A system as claimed in claim 55, wherein the predetermined number is 1.

58. A system as claimed in claim 35, wherein the data lock indicator means is a fixed window phase lock indicator adapted to generate the lock-indicator signal on a basis of a proportion of time, in relation to the predetermined sample period, for which the second beat signal is at a logical-low level.

59. A system as claimed in claim 58, wherein the fixed window phase lock indicator comprises:

a) means for generating a reset signal at a timing of the predetermined sample period; and

b) an N-bit counter adapted to:

i) count bits of the oscillator output signal while the second beat signal is at a logical-low level:

ii) generate an over-flow signal indicative of an over-flow state of the N-bit counter; and

iii) reset a counted number of bits to zero upon receipt of the reset signal.

60. A system as claimed in claim 59, wherein the means for generating a reset signal comprises a 2^M frequency divider adapted to generate the reset signal by frequency-division of the oscillator output signal.

61. A system as claimed in claim 60, wherein values of N and M are selected to provide desired noise-rejection properties of the data lock indicator means.

62. A system as claimed in claim 59, wherein the fixed window phase lock indicator is adapted to assert a value of the lock-indicator signal indicative of an out-of-lock condition when a value of the over-flow signal indicates that the N-bit counter is in an over-flow state, and otherwise assert a value of the lock-indicator signal indicative of an in-lock condition.

63. A system as claimed in claim 62, wherein the fixed window phase lock indicator further comprises:

a) a third digital flip-flop circuit adapted to sample the over-flow signal at a timing of the reset signal; and

b) a logical-NOR gate adapted to assert a value of the lock-indicator signal corresponding to a value of one of the over-flow signal and an output of the third digital flip-flop circuit.

64. A system as claimed in claim 35, wherein the lock detecting means is a sliding window phase lock indicator adapted to generate the lock-indicator signal on a basis of a series of N consecutive samples of the second beat signal.

65. A system as claimed in claim 64, wherein the sliding window phase lock indicator is adapted to assert a value of the lock-indicator signal indicative of an out-of-lock condition if at least 2 out of N+1 consecutive samples of the second beat signal are at a logical low value, and assert a value of the lock-indicator signal indicative of an in-lock condition if at least N consecutive samples of the second beat signal are at a logical high value.

66. A system as claimed in claim 64, wherein the sliding window phase lock indicator comprises:

a) an input digital flip-flop circuit adapted to sample the second beat signal at a timing of a predetermined sample period;

b) an N-bit shift register connected to the input digital flip-flop circuit and adapted to store N consecutive samples of the second beat signal;

c) a first logic gate adapted to assert a high value of a first gate output signal when at least one of the N bits of the shift register, and an

output of the input digital flip-flop circuit are at a low value;

d) a second logic gate adapted to assert a high value of a second gate output signal when all N bits of the shift register are at a high value; and

e) an output digital flip-flop circuit adapted to assert a value of the lock-indicator signal based on the first and second gate output signals.

67. A method of recovering a clock signal from a received data signal, comprising the steps of:

a) sampling the received data signal using a phase detector that generates a phase error signal indicative of a detected phase difference between the data signal and an oscillator output signal, and a digital frequency detector that performs frequency lock on data signal frequencies that fall outside of a pull-in range of the phase detector; and

b) selecting an output of the phase detector when the detected frequency difference is small and otherwise selecting the output of the digital frequency detector to generate the recovered clock signal; and

c) using the selected one of the outputs of the phase detector and the digital frequency detector to control an oscillator to generate the recovered clock signal.

68. A method as claimed in claim 67 wherein selecting an output of the phase detector and the digital frequency detector is performed by a control unit.

69. A method as claimed in claim 67 wherein the digital frequency detector performs the steps of:

a) sampling an in-phase clock at a timing of a data signal to produce a first beat signal;

b) sampling a quadrature clock signal at a timing of the data signal to produce a second beat signal;

c) sampling the second beat signal at a timing of the first beat signal to produce two differential outputs.

70. A method as claimed in claim 69 wherein the two differential outputs determine whether a frequency of the derived clock signal must be increased, decreased or remain unchanged to match a data signal frequency of the received signal.

71. A method as claimed in claim 69 wherein the first beat signal and the second beat signal are used by a data qualification circuit to quantitatively determine a frequency difference between the data signal and the recovered clock signal.

72. A method as claimed in claim 71 wherein transitions of a state of the first and second beat signals are monitored to quantitatively determine a frequency difference between the data signal and the recovered clock signal.

73. A method as claimed in claim 67 wherein operations for recovering the clock signal begin in a reference tracking mode in which the phase detector controls an oscillator to lock to a supplied reference clock, and when a frequency difference between the reference clock and the recovered clock frequency is less than a predetermined threshold, the recovered clock frequency relative to data frequency is monitored.

74. A method as claimed in claim 73 wherein if a difference in the frequency match is smaller than a predetermined threshold, a transition is made to a data tracking mode in which the digital frequency detector controls a frequency of the recovered clock signal to reduce the difference in frequency match between a frequency of the recovered clock signal and a frequency of the data signal.

75. A method as claimed in claim 74 wherein after the digital frequency detector has controlled a frequency of the derived clock signal to an extent that a difference between the frequency of the derived clock signal and the frequency of the data signal is less than the predetermined threshold, control of the derived clock signal is returned to the phase detector.

76. A method as claimed in claim 67 wherein the data signal frequency is known and an appropriate reference clock is supplied, the digital frequency detector providing input to a data qualification circuit that outputs a signal indicative of whether the data received is valid data.

77. A method as claimed in claim 67 wherein clock recovery is performed without a reference clock, comprising the steps of:

a) data frequency acquisition is performed using the digital frequency detector and the recovered clock frequency is adjusted until the frequency is within a pull-in frequency range of the phase detector; and

b) control is switched to the phase detector to lock the frequency of the derived clock signal to the frequency of the data signal.

78. A method as claimed in claim 77 wherein if the lock between the derived clock signal and the data signal is lost, control is again returned to the digital frequency detector to enable the digital frequency detector to re-adjust the frequency of the derived clock signal.